ABSTRACT

A DMA controller includes at least one peripheral DMA channel for handling DMA transfers on a peripheral access bus; at least one memory DMA stream, including a memory destination channel and a memory source channel, for handling DMA transfers on first and second memory access buses; first and second address computation units for computing updated memory addresses for DMA transfers; and first and second memory pipelines for supplying memory addresses to the first and second memory access buses, respectively, and for transferring data on the first and second memory access buses. Channel control logic controls transfer of data through the DMA channels in response to parameters contained in at least one DMA descriptor having a programmable format.